REMARKS

Claims 69-71 have been added. Claims 1-14, 25-31 and 41-71 remain in the application. Reconsideration of the application is requested in view of the amendments and remarks to follow.

Claims 1, 2, 7, 9, 41, 42, 51-57, 62, 63, 66 and 68 stand rejected under 35 U.S.C. §102(e) as being anticipated by Araki et al., U.S. Patent No. 5,882,994. Claims 3-6, 8, 10-14, 25-31, 43-50, 58-61, 64, 65 and 67 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Araki et al., U.S. Patent No. 5,882,994. Applicants traverse for at least the following fifteen reasons.

These reasons are specifically enumerated because the Examiner has stated (p. 3, Office Action dated Oct. 16, 2001) that the Examiner is unable to determine which legal arguments the Examiner has or has not responded to. The Examiner is required to respond to all of these legal arguments in the event that the Examiner persists with the same grounds of rejection. Applicants note in passing that the paragraph by paragraph effort that the Examiner has made missed a number of items and would suggest responding to the arguments as they are enumerated to avoid this situation.

TRAVERSE OF ANTICIPATION REJECTIONS

First, anticipation is a legal term of art. In order to provide a valid finding of anticipation, at least the following components must be

simultaneously satisfied: (i) the reference must include every element of the claim within the four corners of the reference; (ii) the elements must be set forth as they are recited in the claim; (iii) the teachings of the reference cannot be modified; and (iv) the reference must enable the invention as recited in the claim. As will be noted in more detail below, the anticipation rejections fail to establish any of these four conditions. As a result, it is inconceivable that all of these conditions are simultaneously met.

Second, the reference must set forth each and every element of the claim. This is explained in the Manual of Patent Examination Procedure ("MPEP"), as noted below.

For example, the Examiner is referred to MPEP §2131, entitled "Anticipation - Application of 35 U.S.C. 102". This MPEP section states that "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM". This MPEP section elaborates on this, as is explained below in more detail.

This MPEP section states that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)."

Third, the reference must set forth these element of the claim, as the elements are found in the claim. The above-noted MPEP section explains this also, stating that "The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)." This is explained below in more detail with respect to each of independent claims 1, 9 and 51, in subparts A-C.

A. Claim 1 recites "A method for enhancing data retention of a floating gate transistor comprising: forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion", which is not taught or disclosed by Araki et al.

Among other things, Araki et al. do not teach formation of a floating gate transistor. In fact, the term "transistor" occurs only in the Background, at col. 1, lines 33, 36 and 40. Araki et al. teach a nonvolatile semiconductor memory and method of manufacture. Araki et al. are completely silent as to how the memory device might be employed or what elements the floating gate taught by Araki et al. might be combined with to provide a working memory device.

Additionally, Araki et al. do not teach or disclose a "floating gate having an inner first portion and an outer second portion; and providing

conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion". Araki et al. teach formation of a floating gate having three layers, with a first, inner portion being undoped.

Accordingly, Araki et al. do not "set forth each and every element of the claim, as the elements are found in the claim", as is required in order to find anticipation. For at least these reasons, the rejection of claim 1 is prima facie defective and should be withdrawn, and claim 1 should be allowed.

B. The Office Actions fail to even make an effort to show where Araki et al. might provide a teaching of the invention as recited in claim 9. There is no identification anywhere in the Office Actions dated July 7, 1999; November 12, 1999; October 11, 2000; March 27, 2001; May 8, 2001; October 16, 2001; or February 12, 2002 of where Araki et al. might teach or disclose, for example, (i) "forming a first layer of conductively doped semiconductive material over a semiconductive substrate", as recited in claim 9. The commentary on p. 3 of the most recent Action takes the bizarre position that Araki et al. "disclose forming a three layered structure 104" with the first layer being undoped and then equates this to the affirmatively-recited first layer of doped semiconductive material!

Similarly, there is no identification anywhere, in any of these Office Actions, as to where Araki et al. might teach or disclose (ii) "forming a second layer of substantially undoped semiconductive material over the

first layer", as positively recited in claim 9. The Office Action takes the position that three is actually two!

Additionally, there is no identification anywhere, in any of these Office Actions, as to where Araki et al. might teach or disclose (iii) "forming a third layer comprising dielectric material over the second layer", as is positively recited in claim 9. The three layers 106 taught by Araki et al. are unambiguously identified as being atop first, second and third semiconductive layers and a fourth (oxide 105) layer.

Further, there is no identification anywhere, in any of these Office Actions, as to where Araki et al. might teach or disclose (iv) "forming a fourth layer comprising conductive material over the third layer", as is positively recited in claim 9. Given what Araki et al. teach, the layer 107 is thus the eighth layer.

Moreover, there is no identification anywhere, in any of these Office Actions, as to where Araki et al. might teach or disclose (v) "forming a floating gate transistor comprising the first, second, third, and fourth layers", as is positively recited in claim 9.

In the Action dated October 11, 2000, the Examiner states (pp. 2 and 3) that Araki discloses a method of forming a floating gate comprising the steps of forming a polysilicon structure (104) over a semiconductive substrate (101), (104) having a first layer (inner portion - 140 nm thick) and a second layer (outer portion - 70 nm thick). The Examiner is mistaken.

Araki et al. teach (col. 3, lines 20-35) formation of three layers of polysilicon, each 70 nm thick, "such as non-doped polysilicon/impurity doped polysilicon/non-doped polysilicon" (col. 3, lines 23-25; see also Fig. 4). Accordingly, Araki et al. do not teach or disclose elements (i) and (ii) of claim 9 as noted above.

Araki et al. then teach (col. 3, line 46 through col. 4, line 25; see also Fig. 6) formation of a dielectric film 106 on top of the third layer of polysilicon. As a result, it is impossible that Araki et al. teach or disclose "forming a third layer comprising dielectric material over the second layer", as recited in claim 9. Accordingly, Araki et al. do not teach or disclose element (iii) of claim 9.

Araki et al. teach formation of a conductive layer 107 (col. 4, lines 56-58), over the dielectric layer 106/105, which is, in turn, formed atop the three semiconductive layers 104. As a result, Araki et al. do not teach "forming a fourth layer comprising conductive material over the third layer", as recited in element (iv) of claim 9. Accordingly, Araki et al. do not teach or disclose element (iv) of claim 9.

Because Araki et al. fail to teach or disclose elements (i)-(iv), as noted above, it is inconceivable that Araki et al. could teach or disclose element (v), which recites forming a floating gate transistor using elements (i)-(iv). Araki et al. are completely silent as to how the floating gate taught by Araki et al. might be employed and do not teach formation of any

transistor. Accordingly, the anticipation rejection of claim 9 is in error and should be withdrawn, and claim 9 should be allowed.

C. Further, none of the Office Actions show where or how Araki et al. might teach or disclose the invention as recited in claim 51. Claim 51 recites "forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion". As noted above, Araki et al. teach three or more such portions. Claim 51 also recites "providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion', which is not taught or disclosed by Araki et al. Araki et al. teach an inner first portion that is undoped.

Claim 51 also recites "forming the inner first portion in contact with a gate dielectric", which is not taught or disclosed by Araki et al. Araki et al. teach that the inner first portion that is in contact with a gate dielectric is undoped. Claim 51 further recites "forming the outer second portion atop the inner first portion", which is not taught or disclosed by Araki et al. Araki et al. do not teach formation of a second portion having a reduced dopant concentration atop a first, doped portion. Instead, Araki et al. teach forming a doped layer that is "sandwiched" between undoped layers.

For at least these reasons, the anticipation rejection of claim 51 is in error and should be withdrawn, and claim 51 should be allowed.

D. The Office Action also fails to show where Araki et al. might teach or disclose the invention as recited in claim 68. Claim 68 recites,

among other things, "A process for forming a floating gate transistor having enhanced data retention comprising: forming a first layer of conductively doped semiconductive material over a gate dielectric disposed on a semiconductive substrate, the first layer having a dopant concentration of greater than or equal to about 1×10^{18} cm^{-3}; forming a second layer of substantially undoped semiconductive material over the first layer", which is not taught or disclosed by Araki et al. as noted above with respect to claim 51.

Fourth, the teachings of Araki et al. have been consistently mischaracterized in rejecting Applicant's claims. For example, the Examiner states (p. 2, Action dated October 16, 2001; p. 4, Action dated February 12, 2002) that "the doped portion of the polysilicon layer (104) and the underlying portion could be characterized as an "inner first portion" ...." Araki et al. certainly do not make any such characterization.

Araki et al. explicitly state that what is required (col. 3, lines 23-25 and 31-36) is formation of a floating gate comprising three layers, "such as non-doped polysilicon/impurity doped polysilicon/non-doped polysilicon." Araki et al. are unambiguous in their characterization of what they teach.

For further example, the Examiner refers to the Action of May, 2001, for grounds for rejection of claim 51 by reference to the Action dated October 16, 2001. That Action states (p. 2) that "the claims do not require that the inner first portion be uniformly doped." However, Araki et al. do require that the inner first portion be uniformly undoped. Araki et al.

explicitly teach "forming a low impurity density polysilicon layer" as the first layer. Araki et al. explicitly state this in no less than eight places (Abstract; col. 3, lines 22-26, 31-36, 48-53; col. 4, lines 13-17 and 47-50; col. 5, lines 14-17 and 21-25).

Fifth, in the present and previous rejections, the Examiner has admitted that the reference does not set forth the invention as recited in claims 1 and 9, stating (p. 3, Office Action dated October, 2000) that "The first two layers of Araki's floating gate structure can be characterized as one layer."

It is inappropriate to "characterize", or paraphrase, the teachings of a reference in attempting to find anticipation. Such comprises impermissible modification of the teachings of the reference, as set forth above with respect to MPEP §2131 and below with respect to MPEP §706.02. For at least these reasons, the anticipation rejections are in error and should be withdrawn, and claims 1, 2, 7, 9, 41, 42 and 51-57 should be allowed.

Sixth, claim 41, which depends from claim 1, explicitly recites "forming the inner first portion in contact with a gate dielectric; and forming the outer second portion atop the inner first portion". Claim 42, which depends from claim 9, includes recitation that "forming a first layer comprises forming a first layer of conductively doped polysilicon in contact with a gate dielectric layer".

The Examiner's only comments with respect to rejection of claims 41 and 42 are found at p. 2 of an Action dated May, 2001 and these remarks are essentially repeated at p. 4 of the instant Action. These remarks are that "the claims do not require that the inner first portion be uniformly doped." However, the inner first layer recited in claim 41 is explicitly stated in claim 1, from which claim 41 depends, to be doped by "providing conductivity enhancing impurity in the inner first portion".

Applicants note that claim 41 includes the recitation of claim 1, and that claim 42 includes the recitation of claim 9, pursuant to 35 U.S.C. §112, 4TH ¶. This statute states that: "A claim in dependent form shall be construed to incorporated by reference all the limitations of the claim to which it refers." Araki et al. explicitly teach that the inner first layer, in contact with the gate dielectric, be undoped. Accordingly, the rejection of claims 41 and 42 fails to meet the standards for anticipation set forth by law and thus should be withdrawn, and claims 41 and 42 should be allowed.

Seventh, the Office Action of Oct. 2000, as well as the instant Action, state that the first two layers taught by Araki et al. "can be characterized as a single, doped layer." However, Araki et al. teach (col. 3, lines 23-25 and 31-36) formation of a floating gate comprising three layers, "such as non-doped polysilicon/impurity doped polysilicon/non-doped polysilicon."

The Examiner, in the Office Action of Oct. 2000, also states (p. 3) that "Araki [sic] discloses a dopant concentration of $1x10^{20}$ cm^{-3} in the first layer and a dopant concentration of none in the second layer (Col. 5, lines 14-17)." The Examiner is mistaken.

The quoted text is reproduced below:

> In this embodiment, the distribution of impurity density in polysilicon is divided into three layers of non-doped polysilicon layer/polysilicon layer containing phosphorus of about $1x10^{20}$ cm^{-3}/non-doped polysilicon layer.

See also similar text appearing at col. 3, lines 20-25. Simply misreading or misunderstanding what Araki et al. do say fails to transform the teachings of Araki et al. in the manner proposed in the Office Action of Oct. 2000 and incorporated by reference in subsequent Actions. Araki et al. simply do not provide the teachings relied on by the Examiner. For at least these reasons, the rejection of claims 1, 2, 7, 9, 41, 42, 51-57, 62, 63, 66 and 68 is improper and should be withdrawn, and these claims should be allowed.

Eighth, it is impermissible to modify the teachings of a reference in a finding of anticipation. This is articulated at MPEP §706.02.

In a subsection entitled "DISTINCTION BETWEEN 35 U.S.C. 102 AND 103", this MPEP section states that: "The distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present." In other words, no

modification of the teachings of the reference is appropriate in a valid finding of anticipation.

To assist the Examiner further with these concepts, statements appearing in the prosecution history, such as "the doped portion could be considered" followed by a characterization that is completely at odds with the teachings of the reference, constitute modification of the teachings of the reference. Put another way, some modifications may be appropriate in a finding of unpatentability but have no place whatsoever in a finding of anticipation.

Ninth, in order to anticipate, a reference must provide an "enabling disclosure" with respect to the invention as recited in the claim. This is explained in more detail in the Manual of Patent Examination Procedure at §2121.01, entitled "Use of Prior Art in Rejections Where Operability Is In Question". This is explained in more detail below.

This MPEP section states that "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure'...." In re Hoeksema, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). A reference contains an "enabling disclosure" if the public was in possession of the claimed invention before the date of invention."

Araki does not provide an enabling disclosure of the invention as recited in any of these claims, as is evidenced by comparison of what

Araki does in fact teach, the claims and the completely inappropriate mischaracterization of what Araki et al. do in fact teach that is found in the Office Actions.

The Office Action of Oct. 2000 states (p. 2), and this is repeated at p. 4 of the instant action, that the first two layers taught by Araki et al. could be characterized as a single, doped layer. How a reference might or might not be characterized is irrelevant to a finding of anticipation. The reference is considered for what it affirmatively recites within the four corners of the reference.

In this instance, Araki et al. teach (col. 3, lines 23-25 and 31-36) formation of a floating gate comprising three layers, "such as non-doped polysilicon/impurity doped polysilicon/non-doped polysilicon." Araki et al. make no bones about this, and further teach, as noted above, that this is essential.

Applicant's claim 1 recites "forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion".

Additionally, Applicant's claim 9 recites "forming a first layer of conductively doped semiconductive material over a semiconductive substrate; forming a second layer of substantially undoped semiconductive material over the first layer; forming a third layer comprising dielectric

material over the second layer; forming a fourth layer comprising conductive material over the third layer; and forming a floating gate transistor comprising the first, second, third, and fourth layers".

In contrast, Araki et al. teach (Col. 5, lines 14-17) that:

> In this embodiment, the distribution of impurity density in polysilicon is divided into three layers of non-doped polysilicon layer/polysilicon layer containing phosphorus of about $1x10^{20}$ cm^{-3}/non-doped polysilicon layer.

See also similar text appearing at col. 3, lines 20-25. The Examiner is alleging that the three layers of Araki et al. anticipate the recitation of "forming a fourth layer comprising conductive material over the third layer" as recited in claim 9. Araki et al. do not provide a teaching of forming a conductive layer over a dielectric layer. In fact, Araki et al. teach (col. 2, lines 34-41) that such is highly undesirable. Accordingly, Araki et al. do not provide an enabling disclosure of the invention as recited in any of claims 1, 2, 7, 9, 41, 42, 51-57, 62, 63, 66 and 68.

For at least the nine reasons given above, the anticipation rejection of claims 1, 2, 7, 9, 41, 42, 51-57, 62, 63, 66 and 68 is defective and should be withdrawn, and claims 1, 2, 7, 9, 41, 42, 51-57, 62, 63, 66 and 68 should be allowed.

TRAVERSE OF UNPATENTABILITY REJECTIONS

Tenth, claim 25 recites "forming a first layer of polysilicon over a substrate to a first thickness; doping the first layer to a degree sufficient to

define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.; after the doping, forming a second layer of polysilicon over the first layer of polysilicon to a second thickness", which is not taught, disclosed, suggested or motivated by Araki et al.

In contrast, Araki et al. teach (col. 1, lines 56-64) that it is undesirable to form a first layer of a floating gate from doped polysilicon, because then "phosphorus within floating gate 84 is diffused into the cell gate oxide film" and because "it invokes a problem concerning reliability due to an increase in the leak current."

Araki et al. teach that it is undesirable to form a first doped polysilicon layer in forming a floating gate transistor, for reasons noted above. It is a main intent of Araki et al. to provide a first layer that is undoped, and this is done for the intended purpose of separating the doped layer from the gate oxide.

Applicants note that MPEP §2143.01 indicates that "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", and that if the modification does render the prior art unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Modifying the teachings of Araki et al. to try to arrive at the invention as recited in claim 25 clearly defeats a main intent of the teachings of

Araki et al. As a result, there is no motivation, as a matter of law, to modify the teachings of Araki et al. to try to arrive at the invention as recited in claim 25. For at least these reasons, the rejection of claim 25 is improper and should be withdrawn, and claim 25 should be allowed.

Eleventh, Applicants further note the requirements of MPEP §2145(X), entitled "ARGUING IMPROPER RATIONALES FOR COMBINING REFERENCES", section D(2), which states, inter alia, that "It is improper to combine references where the references teach away from their combinations."

Applicants additionally note the requirements of MPEP §2141.02, entitled "Differences Between Prior Art and Claimed Invention", stating that "PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS".

This MPEP section further states that "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)".

The citations from Araki et al. provided above show clearly that Araki et al. teach directly away from the invention as recited in any of Applicants claims. Araki et al. teach that doping of the first layer, that is, the layer immediately atop the gate dielectric, is inappropriate. For at least these

reasons, the rejection of claim 25 is improper and should be withdrawn, and claim 25 should be allowed.

Moreover, if one does, arguendo, assume that it is appropriate to construe the teachings of Araki et al. as suggested in the Office Action, the dopant, which Araki explicitly teaches is contained in the second layer, must somehow be distributed into the first and second layers, with the logical result that the dopant concentration is decreased because it is now spread over a larger volume than is taught by Araki et al. How does the Examiner propose to evaluate the resultant concentration? By what rationale does the Examiner justify this? What teaching is there contained within Araki to provide guidance for these modifications, or to indicate the desirability of making these modifications? The Examiner still has identified no such guidance in Araki et al. for the simple reason that Araki et al. provide no such guidance.

Twelfth, Applicants note the requirements of MPEP §2145, entitled "Consideration of Applicant's Rebuttal Arguments", at subsection X entitled "ARGUING IMPROPER RATIONALES FOR COMBINING REFERENCES" in sub-subsection (B), entitled "Obvious To Try Rationale". This MPEP section states that "An applicant may argue the examiner is applying an improper "obvious to try" rationale in support of an obviousness rejection. "The admonition that 'obvious to try' is not the standard under Section 103 has been directed mainly at two kinds of error."

This MPEP section further states that "In some cases, what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful .... In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." In re O'Farrell, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted) (The court held the claimed method would have been obvious over the prior art relied upon because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful.). See the cases cited in O'Farrell for examples of decisions where the court discussed an improper "obvious to try" approach. See also In re Eli Lilly & Co., 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) and In re Ball Corp., 925 F.2d 1480, 18 USPQ2d 1491 (Fed. Cir. 1991) (unpublished) for examples of cases where appellants argued that an improper "obvious to try" standard was applied, but the court found that there was proper motivation to modify the references."

There is simply no teaching or guidance within Araki et al. to attempt to modify Araki et al. as suggested by the various Office Actions. For at least these reasons, the rejection of claim 25 is improper and should be withdrawn, and claim 25 should be allowed.

Thirteenth, and further, simply stating a conclusion that "it would have been obvious" to combine teachings from references does not meet the standards for a rejection under 35 U.S.C. §103(a) as set forth in The Manual of Patent Examination Procedure at §706.02(j) entitled "Contents of a 35 U.S.C. 103 Rejection." As a result, the proposed combination does not and cannot provide the invention as recited in any of Applicant's claims and thus cannot render Applicant's claims unpatentable. This is described in more detail below with reference to MPEP §2142, entitled "Legal Concept of Prima Facie Obviousness".

This MPEP section states that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. There is no motivation identified anywhere to modify the references to attempt to arrive at the subject matter of Applicant's claims.

This MPEP section also states: "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest **all** the claim limitations."

Since all of the cited references, including the reference relied upon by the Examiner, are silent with respect to a floating gate transistor with the first layer being doped, combining or modifying the teachings of any of the references cannot possibly provide the invention as recited in any of Applicant's claims. Thus, the third prong of the test cannot be met.

As a result, there cannot possibly be a reasonable expectation of success from combining or modifying the teachings of the references, including the reference relied upon. The unpatentability rejection of the claims fails all three components of the test for prima facie obviousness as set forth in the MPEP. For at least these reasons, the rejection of claim 25 is improper and should be withdrawn, and claim 25 should be allowed.

This MPEP section further states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." Since neither of these prongs of the test are met at all, such can hardly be found in the prior art.

Fourteenth, and further, no evidence has been provided as to why it would be obvious to modify the Araki et al. reference. Evidence of a suggestion to combine [or modify] may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing

must be clear and particular. See In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). The Examiner has failed to demonstrate any such evidence. Accordingly, the rejection of claim 25 is defective and should be withdrawn, and claim 25 should be allowed.

Fifteenth, applying the standards for novelty and patentability that the Examiner currently is using, for example, against patents previously issued by the U.S.P.T.O., it is abundantly clear that many of the past U.S. patents would be unpatentable under 35 U.S.C. 102 and/or 103(a) for exactly the same reasons that the instant application has been improperly rejected.

Applicants and their counsel are completely at a loss as to the reasons why the Office has adopted this unprecedented unilateral policy shift. Applicant's counsel has prosecuted hundreds of utility patent applications to completion in the last 10+ years with shorter pendency and with a standard of patentability more reasonable to common sense than the Office is currently insisting on in connection with the present application. Further, the Office is unable to point to any change in the regulations that would permit the Office to take such a drastic change in direction.

For the record therefore, Applicants and their counsel strongly object to this policy shift, and believe that it is clearly contrary to the past practices of the Office; and is unsupported by any legislation. Yet further this policy shift is detrimental both to the Applicants and to the Electronics

Industry as a whole. This shift in Patent Office policy affects U.S. and foreign businesses, inasmuch as foreign manufacturers will be reluctant to bring their new designs to the U.S. if they risk losing control of their designs due to the spurious actions of the U.S. Patent Office.

The Office is unable to point to any change in the regulations under 37 C.F.R.; legislative changes under 35 U.S.C. or any amendments to the MPEP that would permit the Office to take such a drastic change in direction. Consequently, Applicants by and through their attorney state the Office has engaged in a policy shift which violates the provisions of the Federal Constitution regarding Applicants' rights to equal protection under the law.

Dependent claims 2-8, 10-14, 26-31, 41-43, 52-57 and 59-67 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

Additionally, the Examiner's response to argument is deficient in multiple regards. A first deficiency is that the response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §102 (i.e., arguments labeled First through Ninth and Fifteenth), or, in the alternative, is an admission that these rejections are defective. One reason for this is that the Examiner utterly and improperly fails to respond to Applicant's arguments.

Applicants note the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites

37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

Araki et al. teach directly away from the invention as claimed. It is inconceivable that such provides an enabling disclosure of the claimed invention.

Araki et al. teach that the first layer is an undoped layer in contact with the gate dielectric. In fact, such is Araki et al.'s raison d'etre. In other words, the entire point of what Araki et al. teach is that contacting gate dielectrics with undoped polycrystalline silicon provides improved gate characteristics.

A second deficiency is that the even under the unpatentability rejections (i.e., arguments labeled Tenth through Fifteenth), the

combinations fail to provide all of the features recited in any of Applicant's independent claims. The Examiner has ignored these features without providing any appropriate legal basis for doing so.

A third deficiency is the failure to respond to all arguments traversing the unpatentability rejections. Merely repeating that "it would be obvious" to provide the features recited in the claims does not constitute a basis for rejection of the claims.

This is particularly true when, as here, the references fail to provide the features recited in the claims. Additionally, the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

A fourth deficiency is to mischaracterize those arguments that are mentioned in the Action. Representative examples of these deficiencies are previously noted in the prosecution history.

For example, at page 16 of the Response dated January 16, 2002, Applicants point out that Araki et al. fail to teach or disclose "forming a floating gate transistor comprising the first, second, third, and fourth layers", as recited in claim 9.

The Examiner's Response in the Action dated January 16, 2002 is: "With respect to page 16, last paragraph, Araki et al. disclose forming a floating gate." The Office Action fails to note that such does not comprise, describe OR enable formation of a transistor. The Examiner presently states that these recitations are being improperly ignored because they

include preamble language. The case law provided by the Examiner does not support the Examiner's interpretation of these cases. Araki et al. provide no teaching or disclosure of forming source/drain regions, for example, as is affirmatively recited in Applicant's claims.

In other words, the Examiner has simply ignored the fact that Araki et al. do not teach or disclose forming a transistor. Put another way, the Response is completely unrelated to the argument, as well as the subject matter affirmatively recited in the claim.

Another example is found at p. 22, 3RD ¶ and the corresponding "response" at p. 5, 6TH ¶ of the Action dated January 16, 2002 and paraphrased at p. 4 of the present Action: "characterizing" the teachings of the reference in a manner that the reference explicitly teaches away from most certainly does modify the teachings of the reference. Further, this modifies the teachings of the reference in ways that are inappropriate to either anticipation or unpatentability.

A further example is the self-serving assertion (p. 5, last ¶; essentially repeated at p. 6, 5TH ¶, Office Action dated January 16, 2002) that the reference enables the invention because the Examiner rejected the claims! This is not enablement in the sense of 35 U.S.C. §112, as is required for a finding of anticipation. A similarly self-serving assertion appears at p. 6, 6TH ¶.

There is no teaching or guidance anywhere within Araki et al. to attempt to modify Araki et al. as suggested by the Office Action of Oct.

2000 and other Actions. There still is no such teaching or guidance in Araki et al. and the Examiner still has not responded to this argument.

The rejections and responses are clearly erroneous and inappropriate, particularly in view of the fact that the cited reference teaches away from the claimed invention and main intentions of the cited reference are defeated by the combination.

The Examiner has completely and improperly failed to meaningfully respond to Applicant's repeated legal arguments showing this to be the case. In other words, the record is void of any meaningful rebuttal of Applicant's arguments with respect to unpatentability.

For at least these four reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments, that is, each of the arguments herein labeled First through Fifteenth.

Dependent claims 2-8, 10-14, 26-31, 41-43, 52-57 and 59-67 are allowable as depending from allowable base claims and for their own recited features which are neither shown nor suggested by the prior art.

New claims 69-71 are supported at least by text appearing at p. 4, line 5, through p. 9, line 5, of the application as originally filed. No new matter is added by new claims 69-71. New claims 69-71 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes mad** ".

In view of the foregoing, allowance of claims 1-14, 25-31 and 41-71 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Oct. 28, 2002 By: _____

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Reg. No. 36,138

Version with markings to show changes made
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/118,359
Filing Date ..... July 17, 1998
Inventor ..... J. Dennis Keller et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2823
Examiner ..... M. Estrada
Attorney's Docket No. MI22-587
Title: Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors

37 CFR § 1.121(b)(1)(iii) AND 37 CFR § 1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY
RESPONSE TO JULY 26, 2002 FINAL OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Claims

Claims 69-71 have been added.

Because these amendments merely add claims, no amendments involving changes to the application or specification are being made. Accordingly, there are no marked-up versions of claims or specification required or provided.

END OF DOCUMENT